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-/	Application No.	Applicant(s)	
Notice of Allowability	09/818,788	ABDO ET AL.	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.  1. This communication is responsive to amendment filed 9/2/05.			
2. The allowed claim(s) is/are <u>5-10,18-21,23-32 and 36-42.</u>			
3.			
Attachment(s)  1. Notice of References Cited (PTO-892)  2. Notice of Draftperson's Patent Drawing Review (PTO-948)  3. Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date  4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal P 6. ☐ Interview Summary Paper No./Mail Dat 08), 7. ☐ Examiner's Amendn 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), e nent/Comment	,

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### **DETAILED ACTION**

## Allowable Subject Matter

1. Claims 5-10, 18-21, 23-32 and 36-42 allowed.

# Response to Arguments

- Applicant's arguments, see pages 7-11 of amendment, filed 2 September 2005, with respect to claims 29-32 and 36 have been fully considered and are persuasive.
   The 35 U.S.C. 102(e) rejection of claims 29-32 and 36 has been withdrawn.
- 3. Applicant's arguments, see pages 7-11 of amendment, filed 2 September 2005, with respect to claim 37 have been fully considered and are persuasive. The objection of claim 37 has been withdrawn.

## Reasons for Allowance

- 4. The following is an examiner's statement of reasons for allowance:
- 5. Claims 5-10 are allowed because the prior art does not teach "if a request type of the transaction matches a trigger condition, generating a data request, and generating a harassing bus transaction based on the data request."

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6. Claims 18 and 19 are allowed because the prior art does not teach "counting a number of external bus cycles that occur without onset of a new transaction on the external bus, determining if the number meets a threshold value, and if so, generating a harassing transaction on the external bus."

- 7. Claims 20, 21, and 23 are allowed because the prior art does not teach "a validation functional unit block (FUB) having an input coupled to the external bus interface of the data request pipeline, the validation FUB to operate in the domain of the first clock, the validation FUB further comprising: a transaction latch coupled to the external bus interface, and a request library coupled to the transaction latch and having an output coupled to the data request pipeline, to store transaction request types according to an external bus protocol."
- 8. Claims 24-26 are allowed because the prior art does not teach "a bus sequencing unit coupled to the processor core and an external bus, the bus sequencing unit comprising: an arbiter to receive a first data request, a cache memory to store data, and a transaction queue coupled to the arbiter and the cache memory to process the first data request, and a validation functional unit block (FUB) coupled to the bus sequencing unit and the external bus, the validation FUB to receive the first data request from the arbiter to generate a second data request if the first data request matches a triggering condition."

- 9. Claims 27, 28, 38, and 39 are allowed because the prior art does not teach "a bus sequencing unit coupled to the processor core and an external bus, the bus sequencing unit further comprising: an arbiter to receive a first data request, a cache memory to output a hit/miss signal in response to the first data request, and a transaction queue coupled to the arbiter and the cache memory to process the first data request, and a validation functional unit block IFUBI coupled to the bus sequencing unit and the external bus, the validation FUB to receive the hit/miss signal from the cache memory to generate a second data request if the hit/miss signal matches a triggering condition."
- 10. Claims 29-32 are allowed because the prior art does not teach "in response to a the detected transaction, issuing a read request in a second transaction on the external bus, the read request directed to the address read from said first transaction from the external bus."
- 11. Claims 36 and 37 are allowed because the prior art does not teach "storing a request type in a register, observing a transaction on an external bus, and if the request type of the external bus transaction matches the request type stored in the register, generating a data request on the external bus."
- 12. Claims 40-42 are allowed because the prior art does not teach "means for forming a second data request based on the first data address if said means for

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determining determines that the trigger condition is satisfied, and means for posting the second data request to the data bus as a harassing transaction."

13. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

#### Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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JDM September 15, 2005

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